CLAIMS

What is claimed is

1. A crossbar device comprising:

n input lines;

m output lines; and

a plurality of chains of pass transistors, each having a plurality of pass transistors, to seletively couple said n input lines to said m output lines;

where n and m are integers.

2. The crossbar device of claim 1, wherein at least one of the plurality of chains of pass transistors consists of a first and a second pass transitor.

3. The crossbar device of claim 1, wherein each of the plurality of chains of pass transistors consists of a first and a second pass transitor.

4. The crossbar device of claim 1, wherein the device further comprises a plurality of memory elements coupled to the input lines.

5. The crossbar device of claim 1, wherein the device further comprises a plurality p to q decoder logic coupled to the input lines, where p and q are integers, with p being less than q.

6. The crossbar device of claim 1, wherein each of said chains of pass transistors further comprises a memory element coupled to a pass transistor of the chain, disposed on an input side of the chain to control the chain.

7. A reconfigurable circuit comprising:

a plurality of crossbar devices coupled to one another, each crossbar device having at least a memory element, and an output buffer electrically assocaited with the memory element; and

a voltage supply structure coupled to the crossbar device designed to supply Vdd to the output buffers, and a voltage raised by a threshold over Vdd to the memory elements to maintain the input voltage of the output buffers at Vdd.

8. The reconfigurable circuit of claim 7, wherein at least one of the plurality of crossbar devices comrpises

n input line;

m output lines; and

a plurality of chains of pass transistors coupling the n input lines to the m output lines;

where n and m are integers.

9. The reconfigurable circuit of claim 8, wherein at least one of the plurality of chains of pass transistors consists of a first and a second pass transitor.

10. The reconfigurable circuit of claim 8, wherein each of the plurality of chains of pass transistors consists of a first and a second pass transitor.

11. The reconfigurable circuit of claim 7, wherein each of the plurality of crossbar devices comrpises

n input line;

m output lines; and

a plurality of chains of pass transistors coupling the n input lines to the m output lines;

where n and m are integers.

12. The crossbar device of claim 11, wherein each of said chains of pass transistors further comprises a memory element coupled to a pass transistor of the chain, disposed on an input side of the chain to control the chain.

13. The reconfigurable circuit of claim 7, wherein the reconfigurable circuit is an integrated circuit.

14. The reconfigurable circuit of claim 7, wherein the reconfigurable circuit is a block of an integrated circuit.

15. A reconfigurable circuit comprising:

a plurality of crossbar devices coupled to one another, each crossbar device having at least an output buffer; and

a power-on circuitry coupled to the crossbar devices to force the output buffers to a known state at power-on.

16. The reconfigurable circuit of claim 15, wherein the power-on circuitry comprises a flip-flop.

17. The reconfigurable circuit of claim 15, wherein at least one of the plurality of crossbar devices comrpises

n input line;

m output lines; and

a plurality of chains of pass transistors coupling the n input lines to the m output lines;

where n and m are integers.

18. The reconfigurable circuit of claim 17, wherein at least one of the plurality of chains of pass transistors consists of a first and a second pass transitor.

19. The reconfigurable circuit of claim 17, wherein each of the plurality of chains of pass transistors consists of a first and a second pass transitor.

20. The reconfigurable circuit of claim 15, wherein each of the plurality of crossbar devices comrpises

n input line;

m output lines; and

a plurality of chains of pass transistors coupling the n input lines to the m output lines;

where n and m are integers.

21. The crossbar device of claim 20, wherein each of said chains of pass transistors further comprises a memory element coupled to a pass transistor of the chain, disposed on an input side of the chain to control the chain.

22.The reconfigurable circuit of claim 15, wherein

each crossbar device further having at least a memory element electrically associated to an output buffer; and

the reconfigurable circuitr further comprisees a voltage supply structure coupled to the crossbar devices designed to supply Vdd to the output buffers, and a voltage raised by a threshold over Vdd to the memory elements to maintain the voltage supply of the output buffers at Vdd.

23. The reconfigurable circuit of claim 15, wherein the reconfigurable circuit is an integrated circuit.

24. The reconfigurable circuit of claim 15, wherein the reconfigurable circuit is a block of an integrated circuit.